We claim:

1. A support matrix for integrated semiconductors, comprising:

a frame having at least one bonding channel with an edge formed therein, said frame further having a groove formed therein along said edge of said bonding channel;

conductor track structures disposed on said frame, said groove formed in said frame functioning as a barrier for preventing a flow of a flowable material from said bonding channel onto said frame and onto said conductor track structures; and

contacts, selected from the group consisting of bonding leads and wires, connected to said conductor track structures and disposed in said bonding channel, said contacts used for connecting said conductor track structures to an integrated circuit.

2. The support matrix according to claim 1, wherein said barrier is disposed on all sides of said bonding channel and completely surrounds said bonding channel.

3. The support matrix according to claim 1, wherein said frame has a surface remote from said bonding leads and said

barrier is formed in said surface of said frame which is remote from said bonding leads.

4. The support matrix according to claim 1, wherein the flowable material is silicone for forming structures on the support matrix.

5. The support matrix according to claim 1, wherein said barrier has a region with a parting agent disposed thereon for repelling the flowable material.

6. A support matrix for integrated semiconductors, comprising:

a frame having at least one bonding channel with an edge formed therein;

conductor track structures disposed on said frame, said frame and said conductor track structures having a groove formed therein along said edge of said bonding channel, said groove functioning as a barrier for preventing a flow of a flowable material from said bonding channel onto said frame and onto said conductor track structures; and

contacts, selected from the group consisting of bonding leads and wires, connected to said conductor track structures and disposed in said bonding channel, said contacts used for

connecting said conductor track structures to an integrated circuit.

7. The support matrix according to claim 6, wherein said groove is formed to extend into said bonding leads.

8. A method for producing a support matrix for integrated semiconductors, which comprises the steps of:

providing a frame having conductor track structures disposed thereon, at least one bonding channel formed in the frame, and bonding leads disposed in the bonding channel and connected to the conductor track structures for connecting the conductor track structures to an integrated semiconductor; and

forming at least one groove along an edge of the bonding channel for preventing a flow of a flowable material from the bonding channel onto the frame and onto the conductor track structures.

9. The method according to claim 8, which comprises:

applying a resist mask over the frame; and

etching the groove at the edge of the bonding channel.

10. The method according to claim 8, which comprises forming the groove at the edge of the bonding channel using an embossing process.